CLAIMS

What is claimed is:

1. A method of optimizing level converter placement, said method comprising the steps of:

a) selectively placing each level converter at a minimum power point to minimize net power and transitional delay, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter; and

b) eliminating inefficient level converters.

2. A method as in claim 1, wherein at least one said minimum power point is located at a geometric center between a pair of sinks on a corresponding second voltage net.

3. A method as in claim 1, wherein at least one first voltage net originates at a first quadrant and a corresponding second voltage net connects to a plurality of sinks in a second quadrant and said minimum power point is located at minimum horizontal (x) and vertical (y) coordinates of said plurality of sinks.

4. A method as in claim 1 at least one first voltage net originates at a first quadrant and a corresponding second voltage net connects to a plurality of sinks in a second quadrant and wherein said minimum power point is located comprising the steps of:

A) locating a weighted center of said plurality of sinks; and

B) providing a projection from said weighted geometric center to a baseline intersecting one of said plurality of sinks.

5. A method as in claim 4 wherein said baseline is on a diagonal with axes of said second quadrant and said intersecting one is closest to said axes.

6. A method as in claim 4 wherein locating said minimum distance comprises finding a location at a Manhattan distance from a closest one of said plurality of sinks to a source driving said first voltage net.

7. A method as in claim 1, wherein at least one first voltage net originates at a first quadrant and a corresponding second voltage net connects to a plurality of sinks in a second quadrant and third quadrant and said minimum power point is located at a side drive point.

8. A method as in claim 7, wherein said second quadrant and said third quadrant are on one side of an axis, at least one of said plurality of sinks being at a least distance from said axis and said side drive point being located at said least distance directly across said axis from a driver driving said at least one first voltage net.

9. A method as in claim 1, wherein at least one first voltage net originates at a first quadrant and a corresponding second voltage net connects to a plurality of sinks in a second quadrant and third quadrant and said minimum power point is located at a source driving said first voltage net.

10. A method as in claim 1, wherein at said minimum power point is selected to minimize wiring.

11. A method as in claim 1 wherein the step (b) of eliminating inefficient level converters comprises deleting level converter fanin cones below a selected minimum cone size.

12. A method as in claim 1 wherein the step (b) of eliminating inefficient level converters comprises the steps of:

i) defining fanin cones for each of said level converters;

ii) reverting first voltage level nets in fanin cones below a selected minimum fanin size.

13. A method as in claim 12, wherein the step (ii) of reverting voltage level nets comprises:

A) selecting a smallest fanin cone size;

B) reverting said first voltage level nets having said smallest fanin cone size;

C) re-defining said fanin cones;

D) returning to step (A) until said smallest fanin cone size selected in step (A) is said selected minimum fanin cone size.

14. A method as in claim 1 wherein the step (b) of eliminating inefficient level converters comprises the steps of:

i) identifying second voltage level circuit elements receiving inputs from at least two of said level converters;

ii) converting selected ones of said second voltage circuit elements to an equivalent first voltage circuit element;

iii) deleting said at least two level converters; and

iv) inserting a level converter at each output of said equivalent first voltage circuit element.

15. A method as in claim 14, wherein said second voltage circuit elements are selected in step (ii) by checking timing through said equivalent first voltage circuit element and said level converter at each output.

16. A method as in claim 1, wherein the step (b) of eliminating inefficient level converters comprises selectively replacing first voltage level buffer and level converter pairs with a single said level converter, said pairs being one said first voltage level buffer driving a corresponding said level converter.

17. A method as in claim 16, wherein said pairs are selected by checking timing through said single level converter.

18. A method as in claim 1, wherein an input netlist, technology definition and timing constraints are provided for placing and wiring step (a).

19. A method of optimizing level converter placement in a multi supply integrated circuit design, said method comprising the steps of:

a) providing an input netlist, technology definition and timing constraints for a circuit design;

b) selectively placing level converters to minimize net power and transitional delay in said circuit design, each of said level converters being placed at a corresponding minimum power point, transitional delay being a first voltage net delay to a level converter, through said level converter and a second voltage net delay from said level converter; and

c) deleting level converter fanin cones for corresponding said level converters below a selected minimum cone size;

d) converting selected second voltage level circuit elements receiving inputs from at least two of said level converters to an equivalent first voltage circuit element; and

e) selectively replacing first voltage level buffer and level converter pairs with a single said level converter, said pairs being one said first voltage level buffer driving a corresponding said level converter.

20. A method as in claim 19, wherein selectively placing said level converters in step (b) comprises:

i) identifying ones of said level converters driving pairs of sinks on a corresponding second voltage net and locating said minimum power point for said pair at a geometric center between said pair;

ii) identifying first voltage nets originating at a first quadrant with corresponding second voltage nets connecting to a plurality of sinks in a second quadrant and locating said minimum power point in said second quadrant; and

iii) identifying said first voltage nets originating at a first quadrant with a corresponding second voltage net connecting to a plurality of sinks in a second quadrant and third quadrant and locating said minimum power point with said sinks.

21. A method as in claim 20, wherein said minimum power point is located in step (ii) at minimum horizontal (x) and vertical (y) coordinates of said plurality of sinks.

22. A method as in claim 20, wherein, wherein said minimum power point is located in step (ii) comprising the steps of:

A) locating a weighted center of said plurality of sinks; and

B) providing a projection from said weighted geometric center to a baseline intersecting one of said plurality of sinks.

23. A method as in claim 22, wherein said baseline is on a diagonal with axes of said second quadrant and said intersecting one is closest to said axes.

24. A method as in claim 22, wherein locating said minimum distance comprises finding a location at a Manhattan distance from a closest one of said plurality of sinks to a source driving said first voltage net.

25. A method as in claim 20, wherein said minimum power point is located in step (iii) at a side drive point.

26. A method as in claim 25, wherein locating said side drive point comprises:

A) locating an axis between a driver driving a transitional net and sinks on said transitional net;

B) locating at least one of said sinks at a least distance from said axis; and

C) locating a point at said least distance directly across said axis from said driver.

27. A method as in claim 20, wherein said minimum power point is located in step (iii) at a source driving said first voltage net.

28. A method as in claim 19, wherein the step (c) of deleting fanin cones comprises the steps of:

i) defining fanin cones for each of said level converters;

ii) reverting first voltage level nets in fanin cones below a selected minimum fanin size.

29. A method as in claim 28, wherein the step (ii) of reverting voltage level nets comprises:

A) selecting a smallest fanin cone size;

B) reverting said first voltage level nets having said smallest fanin cone size;

C) re-defining said fanin cones;

D) returning to step (A) until said smallest fanin cone size selected in step (A) is said selected minimum fanin cone size.

30. A method as in claim 19, wherein said second voltage circuit elements are selected in step (d) by checking timing through said equivalent first voltage circuit element and said level converters placed at each output.

31. A computer program product for optimizing level converter placement in a multi supply integrated circuit (IC) design, said computer program product comprising a computer usable medium having computer readable program code thereon, said computer readable program code comprising:

computer program code means for locating a minimum power point to minimize power and transitional delay for a level converter placed at said minimum power point, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter

computer program code means for placing level converters at minimum power points; and

computer program code means for eliminating inefficient said level converters.

32. A computer program product as in claim 31, wherein the computer program code means for locating said minimum power point comprises:

computer program code means for locating a geometric center of a plurality of circuit sink elements on a net;

computer program code means for locating a weighted center of said plurality of circuit sink elements on said net; and

computer program code means for determining bounds for said plurality of circuit sink elements on said net.

33. A computer program product as in claim 32, wherein the computer program code means for locating said minimum power point further comprises:

computer program code means for providing a projection from said weighted geometric center to a baseline intersecting one of said plurality of sinks.

34. A computer program product as in claim 33, wherein the computer program code means for locating said minimum power point further comprises:

computer program code means for finding a location at a Manhattan distance from a closest one of said plurality of sinks to a source driving said first voltage net.

35. A computer program product as in claim 31, the computer program code means for eliminating inefficient level converters comprising:

computer program code means for identifying and deleting level converter fanin cones for corresponding said level converters below a selected minimum cone size;

computer program code means for identifying and converting selected second voltage level circuit elements receiving inputs from at least two of said level converters to an equivalent first voltage circuit element; and

computer program code means for selectively replacing first voltage level buffer and level converter pairs with a single said level converter, said pairs being one said first voltage level buffer driving a corresponding said level converter.

36. A computer program product as in claim 35, wherein the computer program code means for locating said identifying and deleting fanin cones comprises:

computer program code means for reverting first voltage level nets in fanin cones below a selected minimum fanin size.

37. A computer program product as in claim 35, wherein the computer program code means for reverting voltage level nets comprises:

computer program code means for selecting a smallest fanin cone size;

computer program code means for reverting said first voltage level nets having said smallest fanin cone size; and

computer program code means for re-defining said fanin cones.

38. A computer program product as in claim 31, further comprising:

computer program code means for receiving an input netlist, technology definition and timing constraints.